

# Self-Heating Aware Logic Cell Design and Optimization

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## Self-Heating 3D TCAD Simulation of Complete Logic Cell

### Layout

GDSII file

### Technology

Description file (ITF-like)

### Layout-based Structure Generation (LSG)

- FEOL (fins with tapered buffers, rounded edges, anisotropic epi blocks)
- BEOL (contacts, interconn.)

### 3D TCAD Model Device Simulation

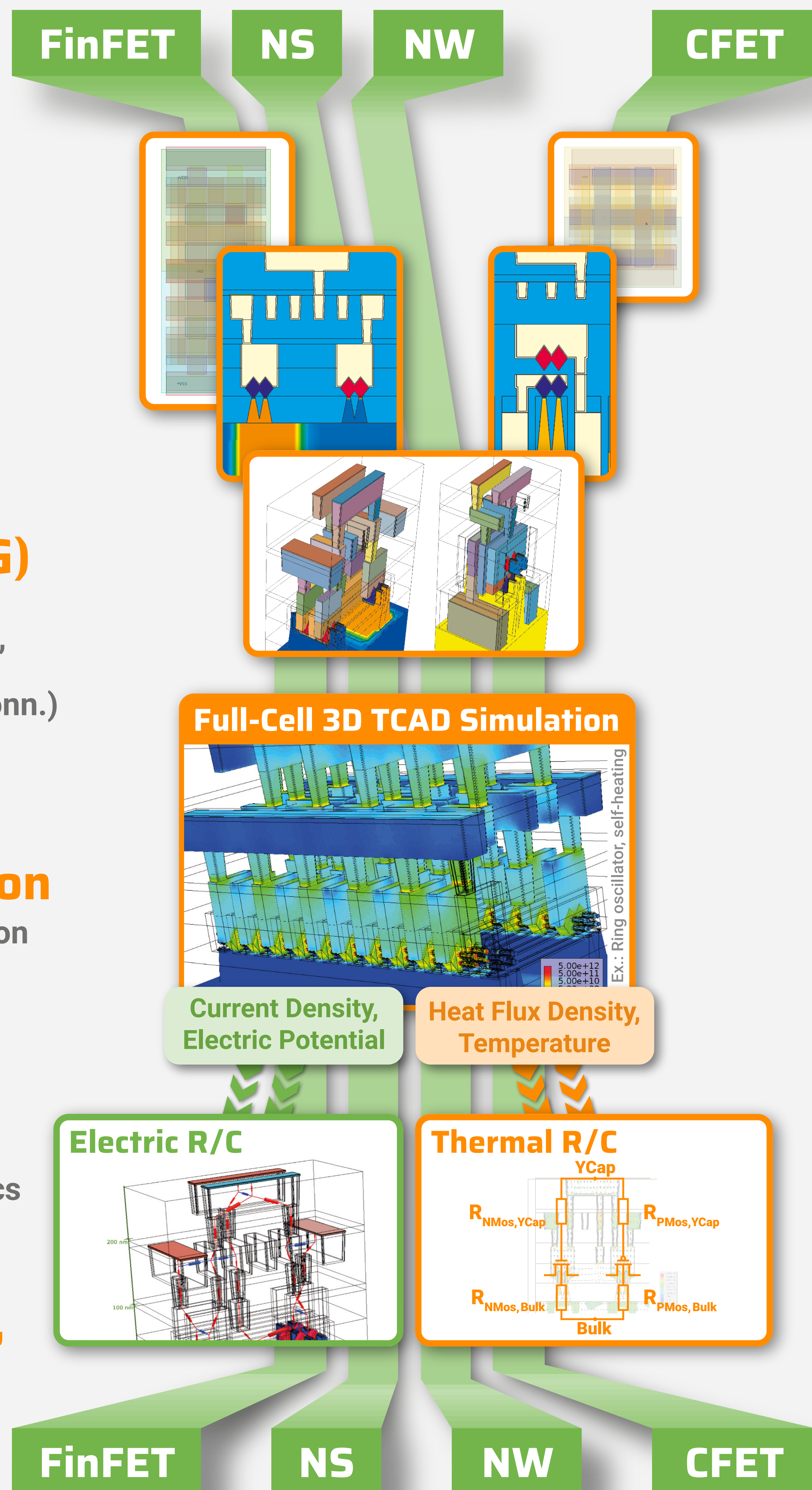
- Full-cell TCAD simulation
- Including self-heating

### R/C Extraction

- Calculate thermal R/C
- Extract electric parasitics

### PPA, Reliability, Temperature

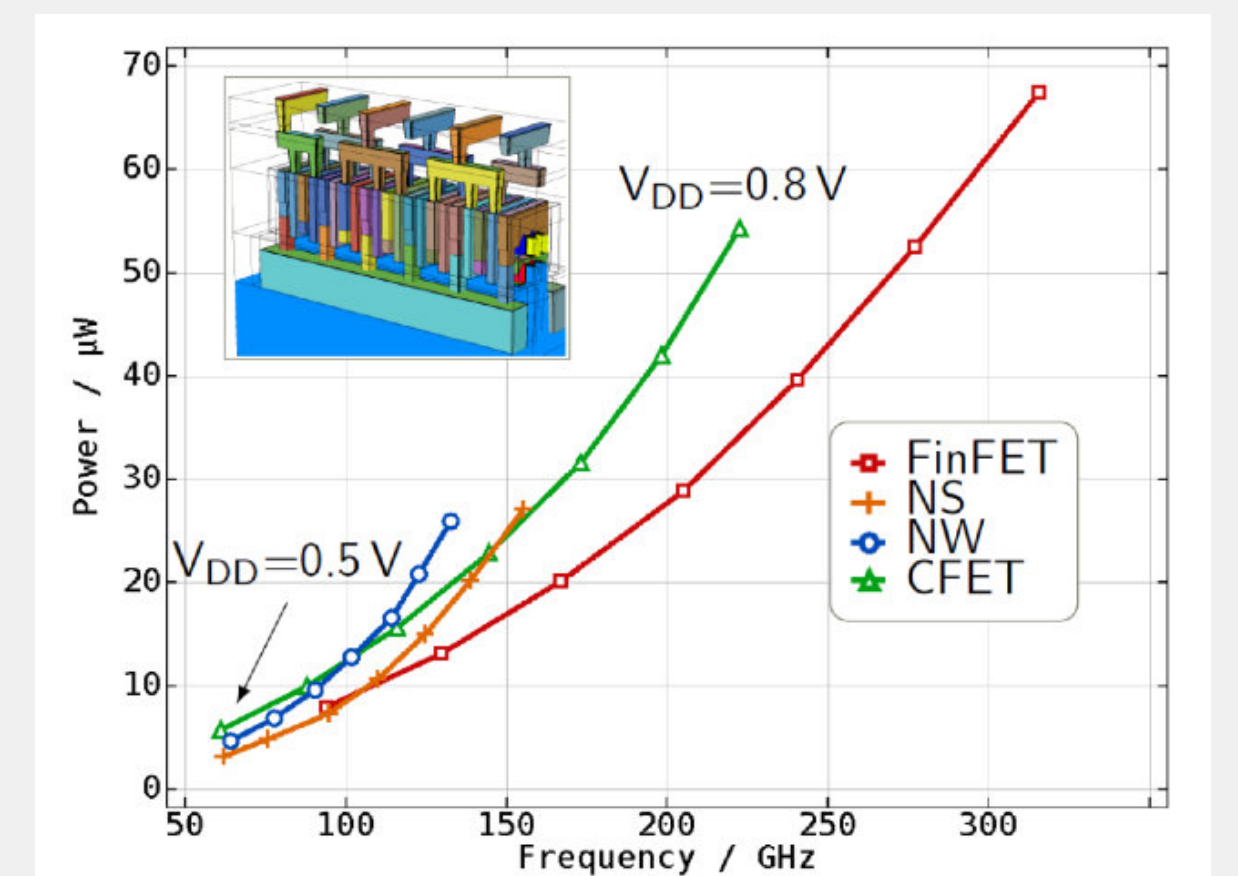
Analyze thermal cell properties, compare designs & technologies



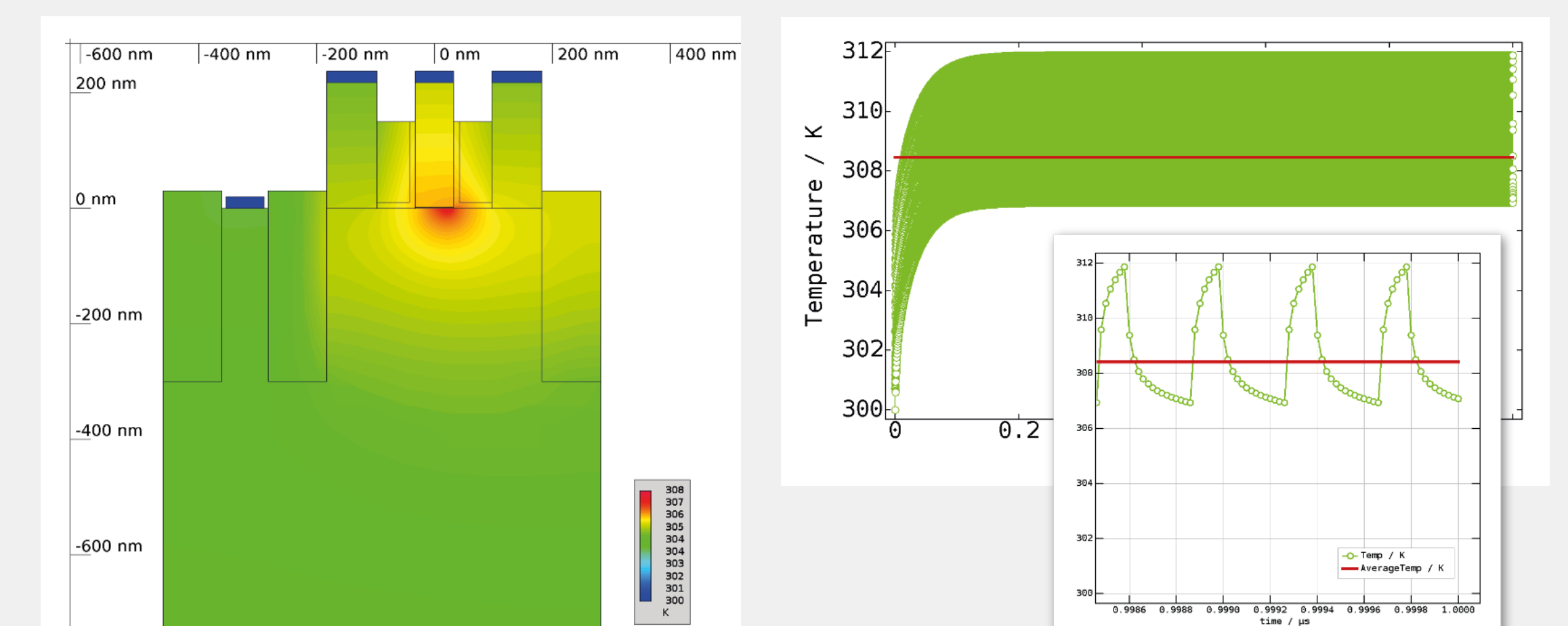
## Incorporating Self-Heating in Cell Design • TCAD DTCO

### Reasoning

- Smaller devices, interactions within cells increase
- Augmenting TCAD-based DTCO (design and technology co-optimization) with thermal awareness is becoming obligatory in cell design

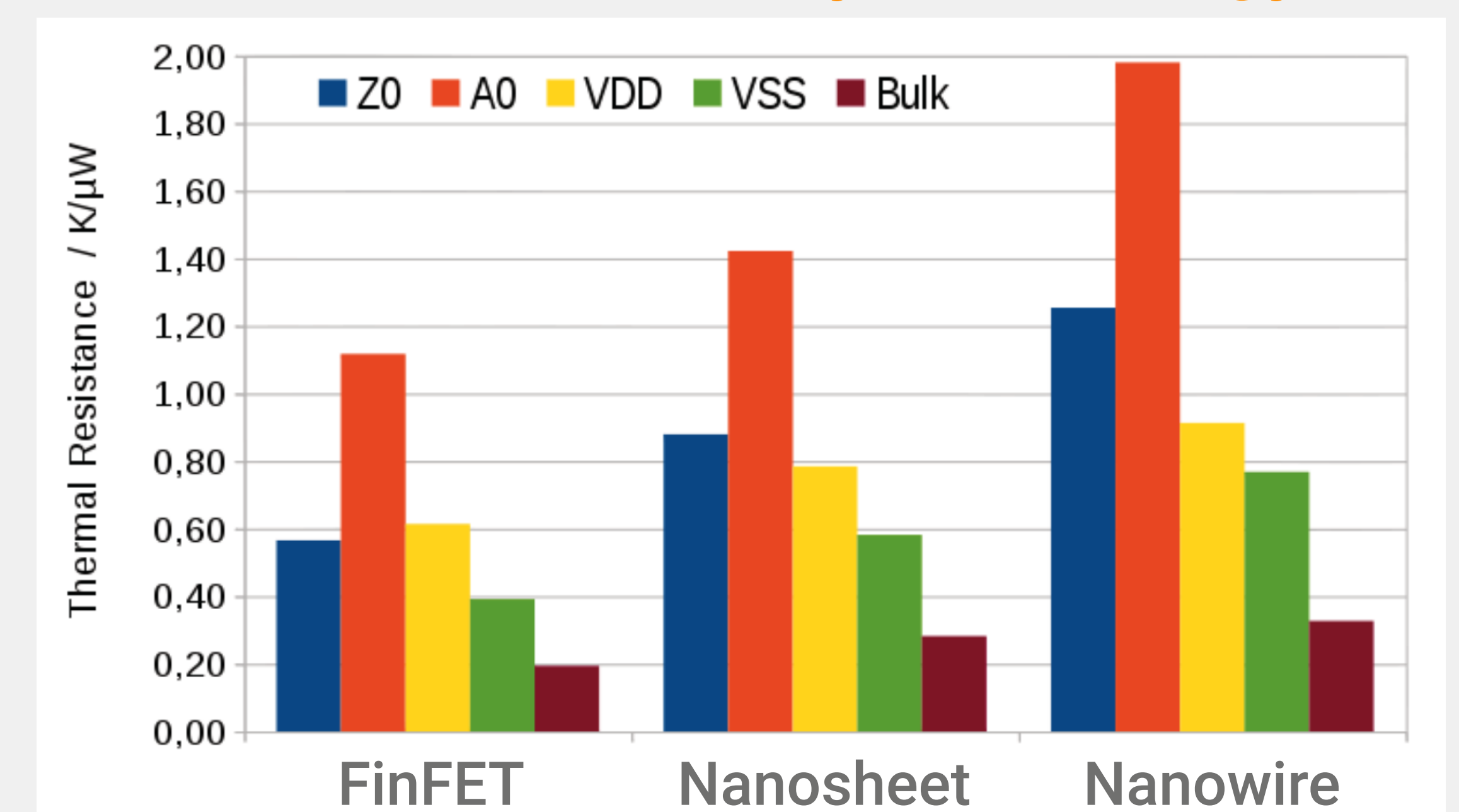


### SH Simulation: Time-Scale Issue

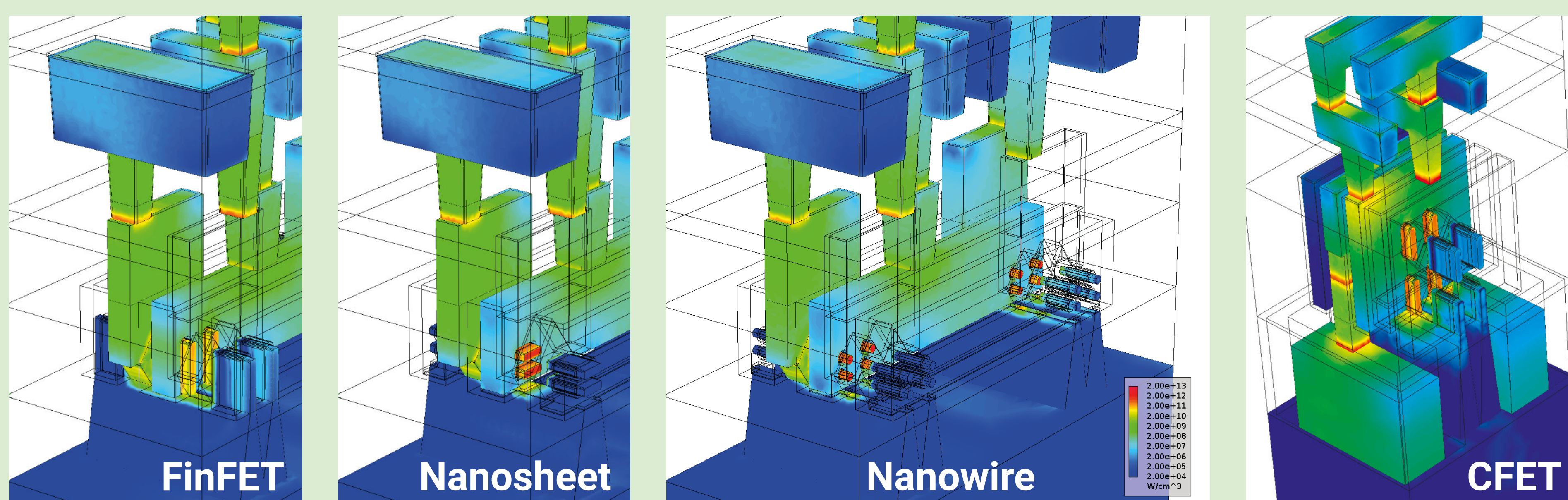


- Average dissipated power of one cycle
- Calculate temperature due to dissipated power
- Verified on 2D MOS full transient thermal profile
- ➔ Capturing the long-term thermal behavior by simulating only one transient cycle

### Thermal Resistance by Technology

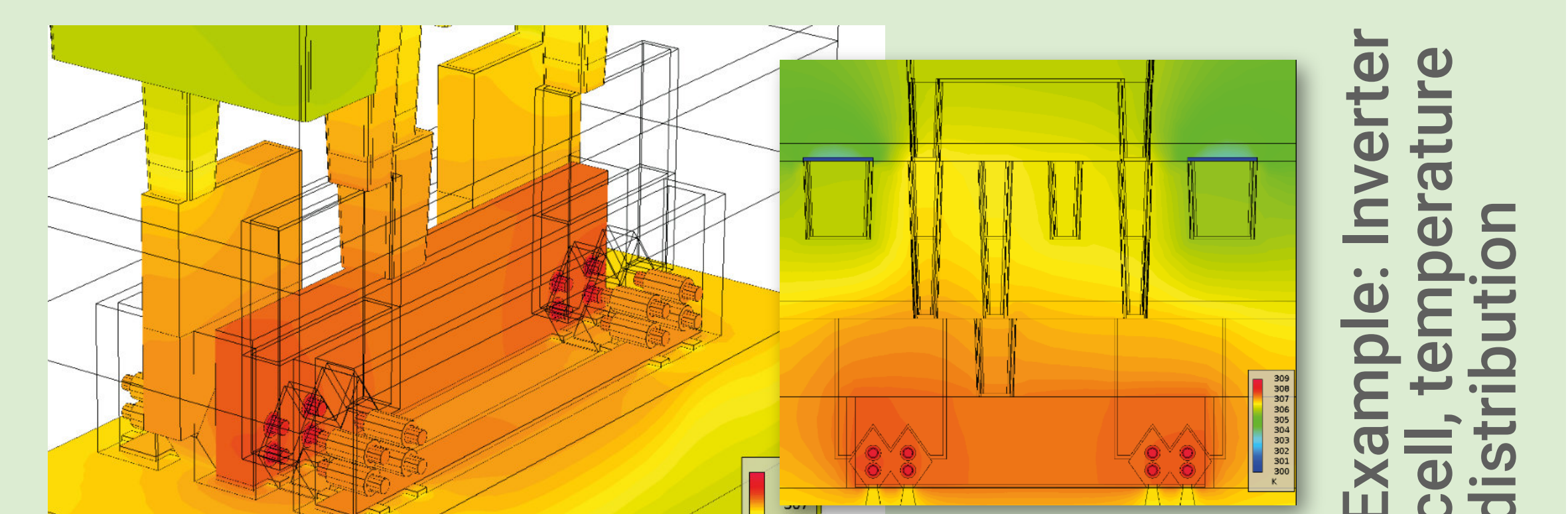


## Results: Technology Comparison



Average heat generation during one full inverter cycle.  
Input for fast temperature profile calculation with various thermal boundary conditions.

## Your Benefit



Example: Inverter cell, temperature distribution

- Identify local thermal hot spots
- at device/cell/block level
- depending on load and layout
- for each specific cell technology